EDP XC167 CPU Module Manual

Version v3.0

This document contains information on the XC167 module for the
RS EDP system

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1. EDP-CM-XC167 CPU Module

The XC167 module uses development tools for C166/XC166 CPUs. The recommended toolchains are
Keil uVISION166 with Keil Compiler for editing and debugging
HitopXC for debugging only. Use Keil uVSION166 for code writing.

Other toolchains may be used such as Tasking but there are no specific examples provided for them.

Keil uVISION166 provides an excellent editor and compilation tool chain for the XC16x family of devices and has been established for a long time. The uVISION166 IDE can also be used as a debugger to program and debug code. Keil uVISION166 has been designed with the ability to talk to the XC167 device over a series of interfaces and JTAG style tools. The XC167 CPU Module has been designed with a USB wiggler chip on board to assist with the programming and debugging of devices.

The user can use Keil uVISION166 for debugging but Hitex has its own debugger called HiTOP XC. This tool is generally not used for editing and code writing but solely for debugging.

If you wish to use the Keil tool for debugging then the key setting in the Keil uVISION166 IDE are as follows.
Select for the debugger as 'Infineon DAS Client for XC167'
In the settings for the debugger then select 'JTAG Over USB Chip'

This should then connect seamlessly to the RS-EDP platform via the mini USB debug connection on the base board.

When using HiTOP XC the connection set up is exactly the same. In either case you do not need to purchase an additional JTAG tool for programming or debugging. It is built in to the module.

2. Get The Latest Versions

Always visit the EDP support website for the latest versions of the tools and examples. This is frequently updated and contains huge amount of useful information. Hitex currently provide an RS-EDP support page and this is on...

www.hitex.co.uk/edp

RS will also provide support for the RS-EDP platform on their own web site. It is envisaged that RS site will replace the Hitex web site and become the sole repository of information on the RS-EDP platform. No URL exists (web address) at the time of writing this manual.

The key documents that are available for the RS-EDP platform are as follow...

- **Spec Sheet**
  This is a single page document detailing the features of the module. Each AM and CM has its own spec sheet.
- **User Manuals**
  A user manual is provided for each module. This is a detailed description of the module, how to configure it plus the circuit diagram and component overlay drawings for that module.
- **Mapping Aid**
  This item describes how the modules interconnect with each other via the backplane. By examining this document it is possible to see at a glance which features of the Applications modules are accessible via the CPU Module.
- **Pin Allocation Spreadsheets**
  This document shows which pins of the MCU are allocated to which function on the RS-EDP

backplane. It details more thoroughly the relationship between the MCU and the Back Plane function than the mapping aid. This document is only available for the CPU Modules

- **Software downloads**
  Example software of using the CPU Module with the other RS-EDP modules.

3. Module Features

XC167 CPU Module	Part Number EDP-CM-XC167
Features	**Comment**
SAF-XC167CI-32F40F, 40MHz CPU	144TQFP pin package,
256k FLASH	
5V operation	
Singe-chip boot but with optional 16 bit external bus	16-bit external multiplexed bus
64kx16, <25ns, 5V SRAM	SRAM mapped to chip select CS1
1x CAN transceiver with PESD2CAN protection	CAN_CTRL
8MHz XTAL 32kHz XTAL for RTC	PLL multiplies to 40MHz
CS8900 Ethernet controller	Easyweb stack
2.5V core regulator	
I2C 3V3 to 5V level shifter	EDP I2C bus is 3V3
FTDI USB-JTAG and ASC1 interface	ASC1 may be connected to a virtual USB COM port via FT2232L
Raw JTAG connector (0.05" socket)	Samtec FTSH
4-DIL switch	Bootstrap, Boot Mode and other configurations
User LED	Yellow (Port 4.3)
Power LED	Blue
ResetIN LED	Orange
ResetOUT LED	Red

4. XC167 To EDP Baseboard Connector Pin Mapping

The XC167 is a high integration MCU device with 144pins. Many of the pins have more than one function for both the MCU and also within the RS-EDP system. This means that not all of the functions are available all of the time and system designer has to take care to ensure the key features of his system are implemented at the expenses of the less important ones. Some compromise has to be made by system user to accommodate the fixed mapping which you see below.

4.1 MCU Pin Mapping

Pin	Pin Name	Comment	RSEDP Name
1	Not connected	Not connected	Not connected
2	Not connected	Not connected	Not connected
3	P20.12/#RSTOUT		#RESOUT
4	#NMI	local pull up	local pull up
5	Vssp		SGND
6	Vddp		5.0V
7	P6.0/#CS0/CC0IO		#CS0
8	P6.1/#CS1/CC1IO	2 hard wired	#CS1
		2 hard wired	EVG8_GPIO56
9	P6.2/#CS2/CC2IO	2 hard wired	#CS2
		2 hard wired	EVG10_GPIO58
10	P6.3/#CS3/CC3IO	2 hard wired	#CS3
		2 hard wired	EVG12_GPIO60
11	P6.4/#CS4/CC4IO		EVG14_GPIO62
12	P6.5/#HOLD/CC5IO	2 hard wired	EVG16_GPIO64
		2 hard wired	GPIO11_I2S_RX_SDA
13	P6.6/#HLDA/CC6IO	2 hard wired	EVG18_GPIO66
		2 hard wired	GPIO13_I2S_TX_CLK
14	P6.7/#BREQ/CC7IO		GPIO15_I2S_TX_SDA
15	P7.4/CC28IO/C		EVM5_GPIO47
16	P7.5/CC29IO/C		EVM4_GPIO45
17	P7.6/CC30IO/C		EVM3_GPIO43
18	P7.7/CC31IO/C		EVM2_GPIO41_CAPADC
19	Vssp		SGND
20	Vddp		5.0V
21	P9.0/SDA0/CC16IO/C		EVG15_GPIO63
22	P9.1/SCL0/CC17IO/C		EVG13_GPIO61
23	P9.2/SDA1/CC18IO/C	2 hard wired	I2C_GEN0_SDA
		2 hard wired	EVG11_GPIO59
24	P9.3/SCL1/CC19IO/C	2 hard wired	I2C_GEN0_SCL
		2 hard wired	EVG9_GPIO57
25	P9.4/SDA2/CC20IO	2 hard wired	CNTRL_I2C_SDA
		2 hard wired	CPU_DACO0_GPIO17
26	P9.5/SCL2/CC21IO	2 hard wired	CNTRL_I2C_SCL
		2 hard wired	CPU_DACO1_GPIO19
27	Vssp		SGND
28	Vddp		5.0V
29	P5.0/AN0		AN0
30	P5.1/AN1		AN1
31	P5.2/AN2		AN2
32	P5.3/AN3		AN3
33	P5.4/AN4		AN4
34	P5.5/AN5		AN5
35	P5.10/AN10/T6EUD		AN10
36	P5.11/AN11/T5EUD		AN11
37	P5.8/AN8		AN8

38	P5.9/AN9		AN9
39	P5.6/AN6		AN6
40	P5.7/AN7		AN7
41	Varef	2 link options	AN_REF
		2 link options	local 5V
42	Vagnd	hard wired	VAGND
		link option	SGND
43	P5.12/AN12/T6IN		AN12
44	P5.13/AN13/T5IN		AN13
45	P5.14/AN14/T4EUD		AN14
46	P5.15/AN15/T2EUD		AN15
47	Vssi		SGND
48	Vddi	local Vreg	local Vreg
49	P2.8/CC8IO/EX0IN		EVG0_GPIO40
50	P2.9/CC9IO/EX1IN		EVG1_GPIO42
51	P2.10/CC10IO/EX2IN		EVG2_GPIO44
52	P2.11/CC11IO/EX3IN		EVG3_GPIO46
53	P2.12/CC12IO/EX4IN		EVG4_GPIO48
54	P2.13/CC13IO/EX5IN		EVG5_GPIO50
55	P2.14/CC14IO/EX6IN	2 hard wired	EVG6_GPIO52
		2 hard wired	EVG19_GPIO67
56	P2.15/CC15IO/EX7IN/T7IN	2 hard wired	EVG7_GPIO54
		2 hard wired	EVG17_GPIO65
57	#TRST	JTAG	local JTAG
58	Vddp		5.0V
59	P3.0/T0IN/TxD1/E	2 link options	ASC1_TX_TTL
		2 link options	local Virtual Comms
60	P3.1/T6OUT/RxD1/E	2 link options	ASC1_RX_TTL
		2 link options	local Virtual Comms
61	P3.2/CAPIN	2 hard wired	IRQ_GPIO16_CNTRL_I2C_INT
		2 hard wired	MOTOR_TCO_FB
62	P3.3/T3OUT		GPIO4_MCI_DAT1
63	P3.4/T3EUD		GPIO6_MCI_DAT2
64	P3.5/T4IN	2 hard wired	IRQ_GPIO18_I2C_GEN0_INT
		2 hard wired	GPIO5_I2S_TX_WS
65	P3.6/T3IN	2 hard wired	IRQ_GPIO20_I2C_GEN1_INT
		2 hard wired	GPIO7_I2S_RX_CLK
66	P3.7/T2IN	2 hard wired	IRQ_GPIO22_I2C_INT
		2 hard wired	GPIO9_I2S_RX_WS
67	P3.8/MRST0		CNTRL_SPI_MRST
68	P3.9/MTSR0		CNTRL_SPI_MTSR
69	P3.10/TxD0/E		ASC0_TX_TTL
70	P3.11/RxD0/E		ASC0_RX_TTL
71	TCK	JTAG	local JTAG
72	TDI	JTAG	local JTAG
73	TDO	JTAG	local JTAG
74	TMS	JTAG	local JTAG
75	P3.12/#BHE/#WRH/E		#WRH
76	P3.13/SCLK0/E		CNTRL_SPI_CLK
77	P3.15/CLKOUT/FOUT		GPIO12_MCI_CMD
78	Vddi	local Vreg	local Vreg
79	Vssi		SGND
80	P4.0/A16		GPIO1
81	P4.1/A17		GPIO3
82	P4.2/A18		CNTRL_SPI_#CS_NSS
83	P4.3/A19	2 hard wired	SPI_SSC_#CS_NSS
		2 hard wired	GPIO14_MCI_PWR
84	P4.4/A20/C	2 link options	CAN0_RX
		2 link options (local Can transceiver)	CANH0

85	P4.5/A21/C		CAN1_RX
86	P4.6/A22/C		CAN1_TX
87	P4.7/A23/C	2 link options	CAN0_TX
		2 link options (local Can transceiver)	CANL0
88	Vddp		5.0V
89	Vssp		SGND
90	P20.0/#RD		#RD
91	P20.1/#WR/#WRL		#WR
92	P20.2/READY	2 hard wired	ASC1_RX_TTL_ASC0_DSR
		2 hard wired	GPIO0
93	P20.4/ALE		ALE
94	P20.5/#EA	local SW400	local DIP switch
95	P0L.0/AD0	2 link options	A0_AD0
		2 link options	GPIO38_AD0
96	P0L.1/AD1	2 link options	A1_AD1
		2 link options	GPIO36_AD1
97	P0L.2/AD2	2 link options	A2_AD2
		2 link options	GPIO34_AD2
98	P0L.3/AD3	2 link options	A3_AD3
		2 link options	GPIO32_AD3
99	P0L.4/AD4	2 link options	A4_AD4
		2 link options	GPIO30_AD4
100	P0L.5/AD5	2 link options	A5_AD5
		2 link options	GPIO28_AD5
101	P0L.6/AD6	2 link options	A6_AD6
		2 link options	GPIO26_AD6
102	P0L.7/AD7	2 link options	A7_AD7
		2 link options	GPIO24_AD7
103	Vddp		5.0V
104	Vssp		SGND
105	P0H.0/AD8	2 link options	A8_AD8
		2 link options	GPIO39_AD8
106	P0H.1/AD9	2 link options	A9_AD9
		2 link options	GPIO37_AD9
107	Not connected	Not connected	Not connected
108	Not connected	Not connected	Not connected
109	Not connected	Not connected	Not connected
110	Not connected	Not connected	Not connected
111	P0H.2/AD10	2 link options	A10_AD10
		2 link options	GPIO35_AD10
112	P0H.3/AD11	2 link options	A11_AD11
		2 link options	GPIO33_AD11
113	P0H.4/AD12	2 link options	A12_AD12
		2 link options	GPIO31_ADI2
114	P0H.5/AD13	2 link options	A13_AD13
		2 link options	GPIO29_AD13
115	P0H.6/AD14	2 link options	A14_AD14
		2 link options	GPIO27_AD14
116	P0H.7/AD15	2 link options	A15_AD15
		2 link options	GPIO25_AD15
117	P1L.0/A0/CC60		MOTORP0L
118	P1L.1/A1/COUT60		MOTORP0H
119	P1L.2/A2/CC61		MOTORP1L
120	P1L.3/A3/COUT61		MOTORP1H
121	P1L.4/A4/CC62	2 hard wired	MOTORP2L
		2 hard wired	EVG20_GPIO69_ASCO_RTS
122	P1L.5/A5/COUT62		MOTORP2H
123	P1L.6/A6/COUT63		MOTORPWM
124	P1L.7/AD7/#CTRAP/CC22IO	3 hard wired	EMG_TRAP

		3 hard wired	EVM10_GPIO68_ASCO_CTS
		3 hard wired	EVM1_GPIO23
125	Vddp		5.0V
126	Vssp		SGND
127	P1H.0/A8/#CC6POS0/CC23IO/E	2 hard wired	EVM0_GPIO21
		2 hard wired	MOTORH0_ENC0
128	P1H.1/A9/#CC6POS1/MRST1	3 hard wired	SPI_SSC_MRST_MISO
		3 hard wired	MOTORH1_ENC1
		3 hard wired	GPIO2_MCI_DAT0
129	P1H.2/A10/#CC6POS2/MTSR1	3 hard wired	SPI_SSC_MTSR_MOSI
		3 hard wired	MOTORH2_ENC2
		3 hard wired	GPIO8_MCI_DAT3
130	P1H.3/A11/SCLK1/E	2 hard wired	SPI_SSC_CLK
		2 hard wired	GPIO10_MCI_CLK
131	P1H.4/A12/CC24IO		EVM9_GPIO55
132	P1H.5/A13/CC25IO		EVM8_GPIO53
133	P1H.6/A14/CC26IO		EVM7_GPIO51
134	P1H.7/A15/CC27IO		EVM6_GPIO49
135	Vddi	local Vreg	local Vreg
136	Vssi		SGND
137	XTAL2	local Xtal	local Xtal
138	XTAL1	local Xtal	local Xtal
139	Vssi		SGND
140	XTAL3	local 32KHz	local 32KHz
141	XTAL4	local 32KHz	local 32KHz
142	#RSTIN		#RESIN
143	#BRKOUT	JTAG	local JTAG
144	#BRKIN	JTAG	local JTAG

4.2 Resources used by MCU Module

The following backplane resources are used by the CPU modules.

Resources Used/Available
5.0V
AN_REF
#RESIN
#RESOUT
SGND
VAGND
AN0
AN1
AN2
AN3
AN4
AN5
AN6
AN7
AN8
AN9
AN10
AN11
AN12
AN13
AN14
AN15
ASC0_RX_TTL
ASC0_TX_TTL

ASC1_RX_TTL
ASC1_TX_TTL
ASC1_RX_TTL_ASC0_DSR
CAN0_RX
CAN0_TX
CAN1_RX
CAN1_TX
CANH0
CANL0
CNTRL_SPI_#CS_NSS
CNTRL_SPI_CLK
CNTRL_SPI_MRST
CNTRL_SPI_MTSR
CPU_DACO0_GPIO17
CPU_DACO1_GPIO19
SPI_SSC_#CS_NSS
SPI_SSC_CLK
SPI_SSC_MRST_MISO
SPI_SSC_MTSR_MOSI
EVG0_GPIO40
EVG1_GPIO42
EVG2_GPIO44
EVG3_GPIO46
EVG4_GPIO48
EVG5_GPIO50
EVG6_GPIO52
EVG7_GPIO54
EVG8_GPIO56
EVG9_GPIO57
EVG10_GPIO58
EVG11_GPIO59
EVG12_GPIO60
EVG13_GPIO61
EVG14_GPIO62
EVG15_GPIO63
EVG16_GPIO64
EVG17_GPIO65
EVG18_GPIO66
EVG19_GPIO67
EVG20_GPIO69_ASCO_RTS
EVM0_GPIO21
EVM1_GPIO23
EVM2_GPIO41_CAPADC
EVM3_GPIO43
EVM4_GPIO45
EVM5_GPIO47
EVM6_GPIO49
EVM7_GPIO51
EVM8_GPIO53
EVM9_GPIO55
EVM10_GPIO68_ASCO_CTS
GPIO0
GPIO1
GPIO2_MCI_DAT0
GPIO3
GPIO4_MCI_DAT1
GPIO5_I2S_TX_WS
GPIO6_MCI_DAT2
GPIO7_I2S_RX_CLK
GPIO8_MCI_DAT3

GPIO9_I2S_RX_WS
GPIO10_MCI_CLK
GPIO11_I2S_RX_SDA
GPIO12_MCI_CMD
GPIO13_I2S_TX_CLK
GPIO14_MCI_PWR
GPIO15_I2S_TX_SDA
GPIO24_AD7
GPIO25_AD15
GPIO26_AD6
GPIO27_AD14
GPIO28_AD5
GPIO29_AD13
GPIO30_AD4
GPIO31_ADI2
GPIO32_AD3
GPIO33_AD11
GPIO34_AD2
GPIO35_AD10
GPIO36_AD1
GPIO37_AD9
GPIO38_AD0
GPIO39_AD8
MOTORP0H
MOTORP0L
MOTORP1H
MOTORP1L
MOTORP2H
MOTORP2L
MOTORH0_ENC0
MOTORH1_ENC1
MOTORH2_ENC2
MOTOR_TCO_FB
MOTORPWM
EMG_TRAP
CNTRL_I2C_SCL
CNTRL_I2C_SDA
I2C_GEN0_SCL
I2C_GEN0_SDA
IRQ_GPIO16_CNTRL_I2C_INT
IRQ_GPIO18_I2C_GEN0_INT
IRQ_GPIO20_I2C_GEN1_INT
IRQ_GPIO22_I2C_INT
#CS0
#CS1
#CS2
#CS3
#RD
#WR
#WRH
ALE
A0_AD0
A1_AD1
A2_AD2
A3_AD3
A4_AD4
A5_AD5
A6_AD6
A7_AD7
A8_AD8

A9_AD9
A10_AD10
A11_AD11
A12_AD12
A13_AD13
A14_AD14
A15_AD15

4.3 Alphabetical Listing of the MCU IO Pins

Pin	Alphabetic Listing of MCU Pins
144	#BRKIN
143	#BRKOUT
4	#NMI
142	#RSTIN
57	#TRST
1	Not connected
2	Not connected
107	Not connected
108	Not connected
109	Not connected
110	Not connected
105	P0H.0/AD8
106	P0H.1/AD9
111	P0H.2/AD10
112	P0H.3/AD11
113	P0H.4/AD12
114	P0H.5/AD13
115	P0H.6/AD14
116	P0H.7/AD15
95	P0L.0/AD0
96	P0L.1/AD1
97	P0L.2/AD2
98	P0L.3/AD3
99	P0L.4/AD4
100	P0L.5/AD5
101	P0L.6/AD6
102	P0L.7/AD7
127	P1H.0/A8/#CC6POS0/CC23IO/E
128	P1H.1/A9/#CC6POS1/MRST1
129	P1H.2/A10/#CC6POS2/MTSR1
130	P1H.3/A11/SCLK1/E
131	P1H.4/A12/CC24IO
132	P1H.5/A13/CC25IO
133	P1H.6/A14/CC26IO
134	P1H.7/A15/CC27IO
117	P1L.0/A0/CC60
118	P1L.1/A1/COUT60
119	P1L.2/A2/CC61
120	P1L.3/A3/COUT61
121	P1L.4/A4/CC62
122	P1L.5/A5/COUT62
123	P1L.6/A6/COUT63
124	P1L.7/AD7/#CTRAP/CC22IO
49	P2.8/CC8IO/EX0IN
50	P2.9/CC9IO/EX1IN
51	P2.10/CC10IO/EX2IN
52	P2.11/CC11IO/EX3IN
53	P2.12/CC12IO/EX4IN

54	P2.13/CC13IO/EX5IN
55	P2.14/CC14IO/EX6IN
56	P2.15/CC15IO/EX7IN/T7IN
90	P20.0/#RD
91	P20.1/#WR/#WRL
92	P20.2/READY
93	P20.4/ALE
94	P20.5/#EA
3	P20.12/#RSTOUT
59	P3.0/T0IN/TxD1/E
60	P3.1/T6OUT/RxD1/E
61	P3.2/CAPIN
62	P3.3/T3OUT
63	P3.4/T3EUD
64	P3.5/T4IN
65	P3.6/T3IN
66	P3.7/T2IN
67	P3.8/MRST0
68	P3.9/MTSR0
69	P3.10/TxD0/E
70	P3.11/RxD0/E
75	P3.12/#BHE/#WRH/E
76	P3.13/SCLK0/E
77	P3.15/CLKOUT/FOUT
80	P4.0/A16
81	P4.1/A17
82	P4.2/A18
83	P4.3/A19
84	P4.4/A20/C
85	P4.5/A21/C
86	P4.6/A22/C
87	P4.7/A23/C
29	P5.0/AN0
30	P5.1/AN1
31	P5.2/AN2
32	P5.3/AN3
33	P5.4/AN4
34	P5.5/AN5
39	P5.6/AN6
40	P5.7/AN7
37	P5.8/AN8
38	P5.9/AN9
35	P5.10/AN10/T6EUD
36	P5.11/AN11/T5EUD
43	P5.12/AN12/T6IN
44	P5.13/AN13/T5IN
45	P5.14/AN14/T4EUD
46	P5.15/AN15/T2EUD
7	P6.0/#CS0/CC0IO
8	P6.1/#CS1/CC1IO
9	P6.2/#CS2/CC2IO
10	P6.3/#CS3/CC3IO
11	P6.4/#CS4/CC4IO
12	P6.5/#HOLD/CC5IO
13	P6.6/#HLDA/CC6IO
14	P6.7/#BREQ/CC7IO
15	P7.4/CC28IO/C
16	P7.5/CC29IO/C
17	P7.6/CC30IO/C
18	P7.7/CC31IO/C

21	P9.0/SDA0/CC16IO/C
22	P9.1/SCL0/CC17IO/C
23	P9.2/SDA1/CC18IO/C
24	P9.3/SCL1/CC19IO/C
25	P9.4/SDA2/CC20IO
26	P9.5/SCL2/CC21IO
71	TCK
72	TDI
73	TDO
74	TMS
42	Vagnd
41	Varef
48	Vddi
78	Vddi
135	Vddi
6	Vddp
20	Vddp
28	Vddp
58	Vddp
88	Vddp
103	Vddp
125	Vddp
47	Vssi
79	Vssi
136	Vssi
139	Vssi
5	Vssp
19	Vssp
27	Vssp
89	Vssp
104	Vssp
126	Vssp
138	XTAL1
137	XTAL2
140	XTAL3
141	XTAL4

4.4 Backplane Signals and Connections

The best place to probe for signals on the backplane is via the breakout connectors ion the base board, P601 to P603.

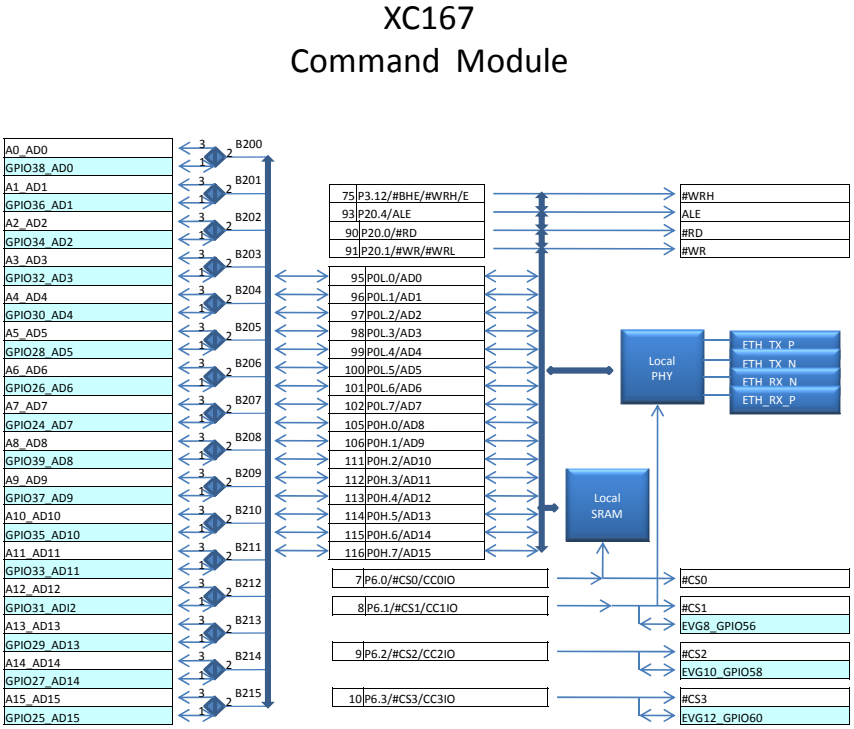
Base Board Signal Name	EDPCON1	EDPCON2	Break Out Connector	
#CS0		53 & 54		
#CS1		55 & 56		
#CS2		57 & 58		
#CS3		59 & 60		
#PSEN		51 & 52		
#RD		45 & 46		
#RESIN		1 & 2	P603	26
#RESOUT		3 & 4	P603	27
#WR		47 & 48		
#WRH		49 & 50		
12V	133		P603	47
12V	134		P603	47
12V	135		P603	47
12V	136		P603	47
12V GND	137		P603	48
12V GND	138		P603	48

12V GND	139		P603	48
12V GND	140		P603	48
3.3V	127		P603	44
3.3V	128		P603	44
3.3V		95 & 96	P603	44
3V BAT	124		P603	42
5.0V	129		P603	45
5.0V	130		P603	45
5.0V		97 & 98	P603	45
A0_AD0		41 & 42		
A1_AD1		39 & 40		
A2_AD2		37 & 38		
A3_AD3		35 & 36		
A4_AD4		33 & 34		
A5_AD5		31 & 32		
A6_AD6		29 & 30		
A7_AD7		27 & 28		
A8_AD8		25 & 26		
A9_AD9		23 & 24		
A10_AD10		21 & 22		
A11_AD11		19 & 20		
A12_AD12		17 & 18		
A13_AD13		15 & 16		
A14_AD14		13 & 14		
A15_AD15		11 & 12		
ALE		43 & 44		
AN_REF	1		P601	6
AN0	3		P603	2
AN1	4		P603	6
AN2	5		P603	1
AN3	6		P603	5
AN4	7		P602	2
AN5	8		P602	4
AN6	9		P602	1
AN7	10		P602	3
AN8	11		P601	2
AN9	12		P601	4
AN10	13		P601	1
AN11	14		P601	3
AN12	15		P603	4
AN13	16		P602	6
AN14	17		P603	3
AN15	18		P602	5
ASC0_RX_TTL	89		P602	30
ASC0_TX_TTL	91		P602	31
ASC1_RX_TTL	93		P602	32
ASC1_RX_TTL_ASC0_DSR	99		P602	35
ASC1_TX_TTL	95		P602	33
ASC1_TX_TTL_ASC0_DTR	97		P602	34
CAN0_RX		61 & 62		
CAN0_TX		63 &64		
CAN1_RX	121		P602	46
CAN1_TX	123		P602	47
CANH0		89 & 90	P603	40
CANL0		91 & 92	P603	41
CNTRL_I2C_SCL		79 & 80	P603	35
CNTRL_I2C_SDA		77 & 78	P603	34
CNTRL_SPI_#CS_NSS		75 & 76	P603	33
CNTRL_SPI_CLK		69 & 70	P603	30
CNTRL_SPI_MRST		71 & 72	P603	31

CNTRL_SPI_MTSR		73 & 74	P603	32
CPU_DAC01_GPIO19	40		P601	7
CPU_DACO0_GPIO17	38		P603	7
EMG_TRAP	114		P601	44
ETH_LNK_LED	111		P602	41
ETH_RX-	109		P602	40
ETH_RX_LED	113		P602	42
ETH_RX+	107		P602	39
ETH_SPD_LED	115		P602	43
ETH_TX-	105		P602	38
ETH_TX+	103		P602	37
EVG0_GPIO40	61		P602	16
EVG1_GPIO42	63		P602	17
EVG2_GPIO44	65		P602	18
EVG3_GPIO46	67		P602	19
EVG4_GPIO48	69		P602	20
EVG5_GPIO50	71		P602	21
EVG6_GPIO52	73		P602	22
EVG7_GPIO54	75		P602	23
EVG8_GPIO56	77		P602	24
EVG9_GPIO57	78		P601	26
EVG10_GPIO58	79		P602	25
EVG11_GPIO59	80		P601	27
EVG12_GPIO60	81		P602	26
EVG13_GPIO61	82		P601	28
EVG14_GPIO62	83		P602	27
EVG15_GPIO63	84		P601	29
EVG16_GPIO64	85		P602	28
EVG17_GPIO65	86		P601	30
EVG18_GPIO66	87		P602	29
EVG19_GPIO67	88		P601	31
EVG20_GPIO69_ASCO_RTS	92		P601	33
EVM0_GPIO21	42		P601	8
EVM1_GPIO23	44		P601	9
EVM2_GPIO41_CAPADC	62		P601	18
EVM3_GPIO43	64		P601	19
EVM4_GPIO45	66		P601	20
EVM5_GPIO47	68		P601	21
EVM6_GPIO49	70		P601	22
EVM7_GPIO51	72		P601	23
EVM8_GPIO53	74		P601	24
EVM9_GPIO55	76		P601	25
EVM10_GPIO68_ASCO_CTS	90		P601	32
GPIO0	21		P603	13
GPIO1	22		P603	15
GPIO2_MCI_DAT0	23		P603	14
GPIO3	24		P603	16
GPIO4_MCI_DAT1	25		P603	17
GPIO5_I2S_TX_WS	26		P603	19
GPIO6_MCI_DAT2	27		P603	18
GPIO7_I2S_RX_CLK	28		P603	20
GPIO8_MCI_DAT3	29		P603	22
GPIO9_I2S_RX_WS	30		P603	21
GPIO10_MCI_CLK	31		P603	23
GPIO11_I2S_RX_SDA	32		P603	24
GPIO12_MCI_CMD	33			
GPIO13_I2S_TX_CLK	34		P603	25
GPIO14_MCI_PWR	35		P603	12
GPIO15_I2S_TX_SDA	36		P603	8
GPIO24_AD7	45		P602	8

GPIO25_AD15	46		P601	10
GPIO26_AD6	47		P602	9
GPIO27_AD14	48		P601	11
GPIO28_AD5	49		P602	10
GPIO29_AD13	50		P601	12
GPIO30_AD4	51		P602	11
GPIO31_ADI2	52		P601	13
GPIO32_AD3	53		P602	12
GPIO33_AD11	54		P601	14
GPIO34_AD2	55		P602	13
GPIO35_AD10	56		P601	15
GPIO36_AD1	57		P602	14
GPIO37_AD9	58		P601	16
GPIO38_AD0	59		P602	15
GPIO39_AD8	60		P601	17
I2C_GEN0_SCL		7 & 8	P603	29
I2C_GEN0_SDA		5 & 6	P603	28
I2C_GEN1_SCL	119		P602	45
I2C_GEN1_SDA	117		P602	44
IRQ_GPIO16_CNTRL_I2C_INT	37		P603	11
IRQ_GPIO18_I2C_GEN0_INT	39		P603	10
IRQ_GPIO20_I2C_GEN1_INT	41		P603	9
IRQ_GPIO22_I2C_INT	43		P602	7
MOTOR_TCO_FB	122		P601	48
MOTORH0_ENC0	116		P601	45
MOTORH1_ENC1	118		P601	46
MOTORH2_ENC2	120		P601	47
MOTORP0H	102		P601	38
MOTORP0L	100		P601	37
MOTORP1H	106		P601	40
MOTORP1L	104		P601	39
MOTORP2H	110		P601	42
MOTORP2L	108		P601	41
MOTORPWM	112		P601	43
SGND	131		P603	46
SGND	132		P603	46
SGND		9 & 10	P603	46
SGND		99 & 100	P603	46
SPI_SSC_#CS_NSS	101		P602	36
SPI_SSC_CLK	98		P601	36
SPI_SSC_MRST_MISO	94		P601	34
SPI_SSC_MTSR_MOSI	96		P601	35
USB_DEBUG_D-		67 & 68		
USB_DEBUG_D+		65 & 66		
USB_DEV_D-		87 & 88	P603	39
USB_DEV_D+		85 & 86	P603	38
USB_HOST_D-		83 & 84	P603	37
USB_HOST_D+		81 & 82	P603	36
VAGND	19		P601	5
VAGND	20		P601	5
Vcc_CM	125		P603	43
Vcc_CM	126		P603	43
Vcc_CM		93 & 94	P603	43

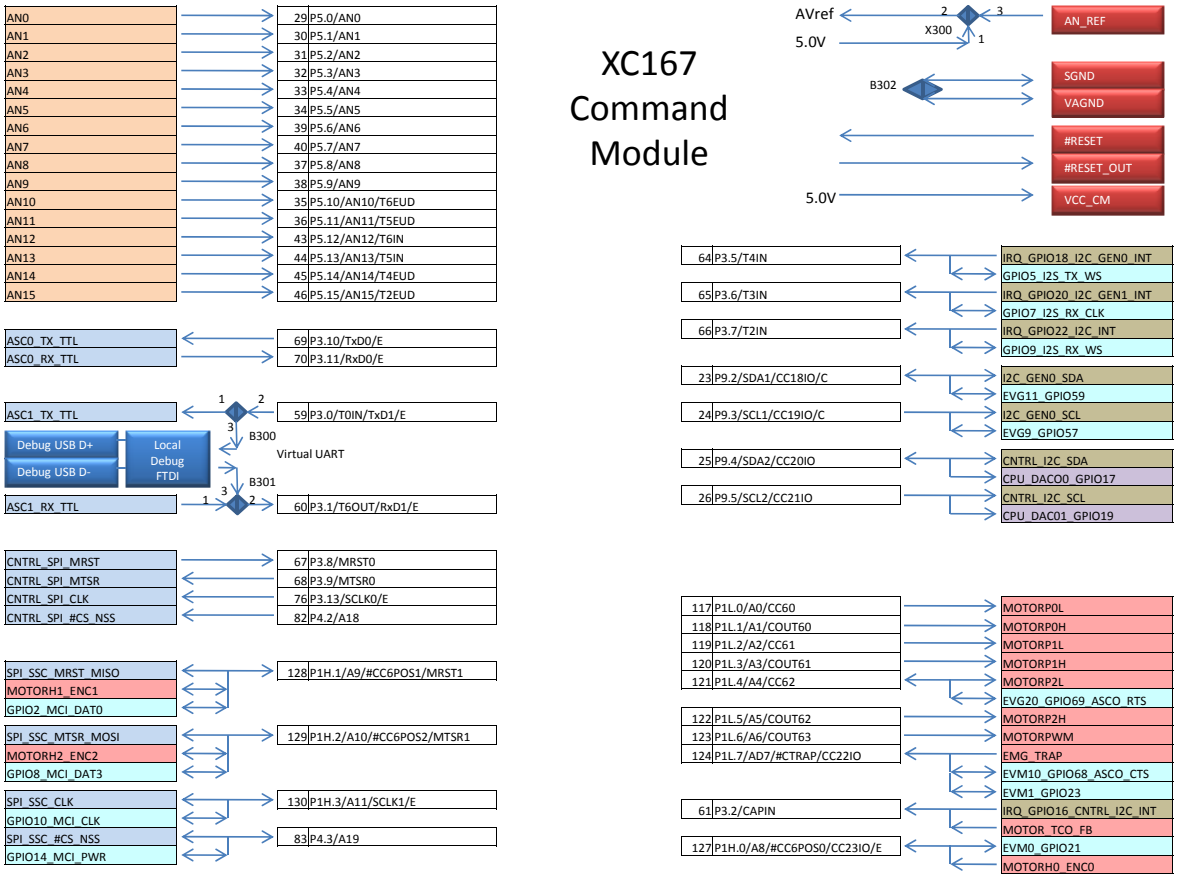
4.5 Mapping Aids



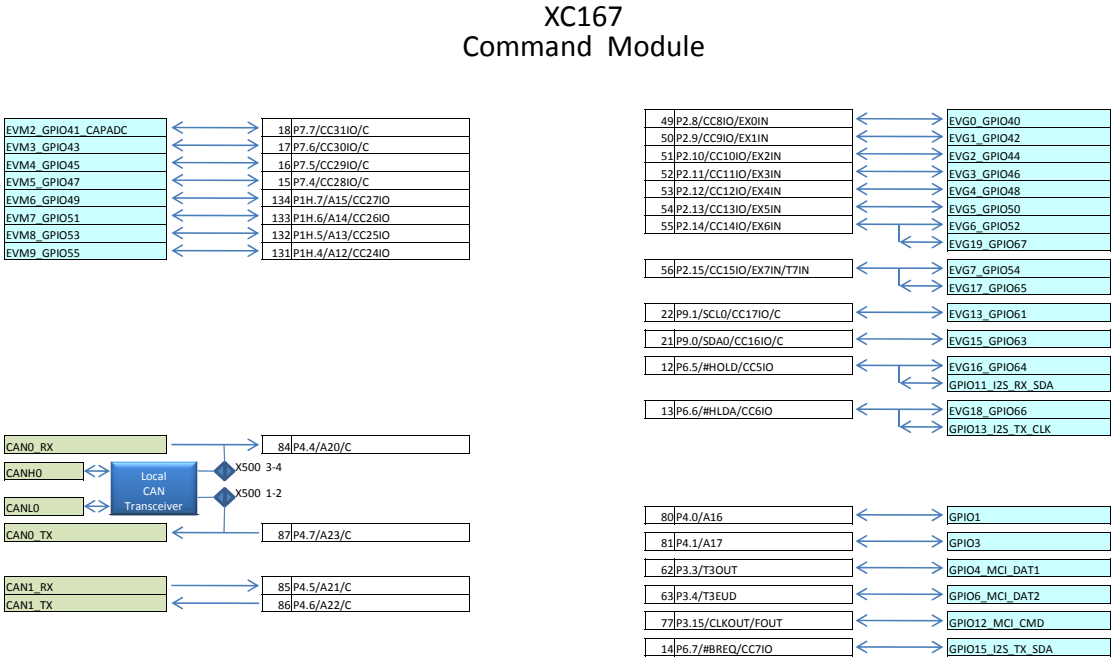
XC167 Mapping Aid

The external bus of the XC167 is used to address the external SRAM and the external Ethernet controller. The provided software configures the CPU Module for use with external memory devices and as such the external bus is live. The key MCU pins are detailed above and show how the SRAM and Ethernet controller are being controlled. The user can elect if he so wishes to have the external bus bought out on to the EDPCON2 connector and all of the bus control signals, address and data lines made available. This would normally only be done if a module has been designed that sits in another base board position that requires access to this bus. None of the basic Application Modules currently require this bus.

Note: If the user wishes to use the GPIO24 – GPIO39 lines as general purpose IO then the bus should be deselected in the user software and the link options be set to the 1-2 position. The user must also note that the SRAM and the PHY are still connected to the IO pins of the MCU even if the jumper options are in the 1-2 position. The user should therefore manage the CS0 and CS1 signals to these devices and ensure they remain in a high state to ensure the device are deselected and do not cause contention of the IO lines.



The user has the ability to select a virtual communication port and can route serial traffic away from ASC1_TX_TTL and ASC1_RX_TTL to the virtual communication port provided by the local FTDI debug chip. This serial traffic uses the same USB cable as the debugger and appears on the PC as a new COMM port. The new COMM port is recognised as soon as the debug USB cable is plugged in to the base board.



The CAN peripheral can route traffic via the on board local CAN transceiver or via the CAN transceiver on the Communications module. See jumper settings below for detailed explanation.

5. XC167 Module Selectable Jumpers

The XC167 module has the following selectable options:

Option	Type	Purpose	Default	Notes
B200-B215	Solder bridge	Connect CPU P9 & P8 multiplexed address bus to EDPCON2 or EDPCON1	Connect to EDPCON1 for IO use (XC167 bus isolated from backplane)	1-2 position – the bus lines can be used as general purpose IO addressing GPIO24-GPIO39 2-3 position – bus external bus is made available on EDPCON2
B300-B301	Solder bridge	Connect ASC1 to USB virtual COMport	Connect ASC1 to EDPCON1	1-2 position allows XC167 ASC1 to be used as a standard serial port 2-3 position allows XC167 ASC1 to be routed to a COMport on PC without using RS232 via FTDI chip.

X300	Jumper	Select source of analog reference voltage	Reference derived from local 5V	1-2 position – selects the local 5.0V supply to be the voltage reference source for the analogue circuitry. 2-3 – position – selects the external ANREF signal from the back plane. This is normally provided by the analog module. The EDP-AM-AN16 module required to use external reference
SW400	DIL Switch	Select XC167 boot configuration	Set internal FLASH boot	See XC167 User Manual for details
X500	Jumper	Enable local CAN transceiver on CAN0	Enabled	1-2 shorted and 3-4 shorted to use the local CAN transceiver. 1-2 open and 3-4 open to use the CAN transceiver on the Communications Module. See section below for dual CAN
B302	Zero ohm link	To connect the analog ground and the signal ground lines to gether.	connected	Inserted – this shorts the analog ground used for on board ADC measurement to the digital signal ground. Removed – the two grounds are not connected. The user will need to short both grounds together at some locations within the RS-EDP system. This can be done on the base board, or on the analogue module if it is not done here.

The default jumper settings will cover most situations.

5.1 B200-B215 External Bus Solder Bridges

The external bus on the XC167 MCU is made available to a local on board SRAM device and Ethernet controller. By default the boards are populated with both the SRAM and Ethernet controller and so the provided software is configured to address the external bus. The two devices are always connected to the bus of the MCU irrespective of the positions of the B200-B215 solder bridges. This means the user must manage the chip select CS0 and CS1 lines carefully as if the user does not intend to use the SRAM at all, it must be made inert by ensuring the CS0 and CS1 line remains high. Both of the CS line can be used as a general purpose IO line if the external bus is not setup in software.
When the external bus is in use, the user can elect if he so wishes to make all of the necessary address, data and bus control signals, available on the EDPCON2 bus. To do this the user must ensure the solder bridges are in the 2-3 positions and the shorting links between positions 1-2 are cut. The user should only ever do this if he has designed his own module that required this external bus to be made available to him. Under normal operation the user would not do this as none of the basic EDP Application Modules require the external bus.
By leaving the shorting links in position 1-2 which is the default position the STR9 can effectively use some of the other backplane resources as general purpose IO. (assuming the external bus is not configured in software).

5.2 B300 and B301 Virtual Communications Port

B300 and B301 control the ASC1_Tx and ASC1_Rx signals respectively to the virtual communication port made available through the on board FTDI chip. This chip is used as a bridge between the IDE (Keil uVISION166 or HiTOP) and the XC167 device and provides support for programming and debugging. The FTDI chip has an additional function also in so much as it has a virtual communication port. The user can elect to stream RS232 TTL traffic via this interface thereby allowing the user to receive standard RS232 terminal traffic via the mini USB socket on the Base Board. To enable the virtual comm. port setting the user bust select options 2-3 for both B300 and B301.

The virtual communication port will require the installation of a virtual comms port driver for the FTDI chip. This should be part of the uVISION166/HiTOP installation which uses the FTDI as a debugger/wiggler.

5.3 X300 Analog Reference Voltage

The on board A to D converter (ADC) can make use of an external stable voltage to better achieve higher accuracy results. The user has the option to select between the external ANREF signal present on the RS-EDP backplane or the local 5.0V supply of the MCU.
The AN16 Analogue module can provide either a 5.0V voltage reference or a 3.3V voltage reference (link option on the analog module) both provided from stable voltage reference devices. If the Analog Module is not fitted the user can elect to use a local 5.0V voltage source instead.

5.4 XC167 Module DIL Switch Settings

The XC167 has 4 DIL switches (SW400) which are used to configure the startup of the XC167 CPU. The switches are by default set to standard internal FLASH start mode (#EA=1) and it is likely that this would ever need to be changed. The most important is switch is “1” which when set to ON will enable the built-in serial bootstrap mode via ASC0. Setting switch “3” to on as well will cause the CAN bootstrap loader to be enabled.

5.4.1 Entering The Special Bootstrap Modes

To enter bootstrap mode, set the switch 1 to ON and then power up the EDP baseboard or press the RESET button. Tools such as the Infineon MEMTOOL can then be used to program the on-chip FLASH.

5.5 X500 Local CAN Transceiver

The twin CAN peripherals on the XC167 device outputs TTL level traffic, CAN0_TX, CAN0_RX and CAN1_TX, CAN1_RX. This TTL traffic is routed down the backplane to the Communications Module. If the user wants an isolated CAN solution he can select via jumper options on the Communication Module to select either CAN0 or CAN1 signals. The isolated physical layer CAN output is via a pin header on the Communication Module.

In addition to this the user can optionally select the CAN1 traffic to routed via the on board local CAN transceiver on the STR9 CPU Module. The local CAN transceiver outputs its physical layer traffic called CANH and CANL down the back plane. This is also picked up on the Communication Module where the traffic exits the Application Module (AN) via the 9 way connector.

The user cannot use CAN1 for both isolated CAN and the local transceiver device at the same time as there will effectively be two CAN_RX signals which will contend with each other. The user must therefore select between isolated CAN, in which case the CAN transceiver on the Communications module is used, or the non isolated CAN in which case transceiver on the CPU Module is used. The user must therefore select the jumper options with care on both the XC167 Module and the Communications Module.

It is possible to have a twin CAN solution with CAN0 taking the isolated traffic route and CAN1 taking the local transceiver route.

For single CAN operation using CAN0

To select the non isolated CAN solution using the local CAN transceiver the user must select X500 position 1-2 shorted and position 3-4 shorted.
Communication Module – P205 – all jumpers removed

For isolated CAN using the CAN transceiver on the Communications Module the user must select
X500 – all jumpers removed
Communications Module – P205 1-3 shorted and 4-6 shorted

For Dual CAN operation
CAN0 is the non isolated CAN
CAN1 is the isolated CAN
X500 position 1-2 shorted and position 3-4 shorted.
Communication Module – P205 3-5 shorted and 2-4 shorted

5.6 B302 Zero Ohm Link - Analog Grounding Arrangements

The analog ground (Avref) pin on the XC167 CPU is not connected to the digital ground on the module itself as they are separated by the B302 zero ohm link. For normal operation this link should be closed. The analog signal ground and the digital signal ground are effectively at the same level and this is the desired arrangement for best noise performance. The analogue module also has the capability of shorting the two grounds together also.